CLAIMS

What is Claimed is:

1. A method of making a hermetically sealed, wafer level chip scale package, comprising the steps of:

(A) providing a cap for protectively covering active areas on the chip;

(B) applying a layer of metalization on one face of the cap;

(C) forming a continuous bead of solder completely surrounding the active chip area;

(D) assembling the cap and the chip with the solder bead positioned between and contacting the metalization layer and the area on the chip surrounding the active chip area; and,

(E) melting the solder bead to form a continuous, hermetic seal around the active chip area between the cap and the chip.

2. The method of Claim 1, wherein step (C) includes forming the solder bead on the face of the cap having the layer of metalization.

3. The method of Claim 2, wherein step (C) includes:

applying a pattern mask over the metalization layer,

applying a layer of solder through the mask onto the metalization layer.

4. The method of Claim 3, wherein applying the pattern mask includes depositing a layer of photoresist over the metalization layer, exposing and developing the photoresist, and stripping exposed areas of the photoresist to achieve a desired mask pattern.

5. The method of Claim 1, wherein step (C) includes an electroplating process step.

6. The method of Claim 1, wherein step (C) includes:

forming a photoresist pattern mask over the metalization layer,

electroplating a layer of solder material through the mask onto the metalization layer, and

striping away the photoresist pattern mask.

7. The method of Claim 6, wherein step (C) includes reflowing the solder layer to form the solder bead.

8. The method of Claim 7, including the steps of:

bonding a spacer onto the cap, and

after step (E) is performed, cutting away a portion of the cap that includes the spacer.

9. The method of Claim 1, including the step of forming a spacer on the cap, and wherein:

step (C) is performed by electroplating a layer of solder through a pattern mask onto the metalization layer,

step (D) includes bringing the spacer into face-to-face contact with chip, and

after step (E) is performed, cutting away a portion of the cap to which the spacer is bonded.

10. A wafer level chip scale package produced by the method of Claim 1.

11. A wafer level chip scale package produced by the method of Claim 9.

12. A method of making a hermetically sealed, wafer level chip scale package, comprising the steps of:

(A) providing a semiconductor wafer having a plurality of chip portions formed therein, said wafer having a first face and a second opposite face,

(B) providing a cap for protectively covering active areas on each of the chip portions;

(C) applying a layer of metalization on one face of the cap;

(D) applying a plurality of continuous, patterned beads of solder to the metalization layer;

(E) bringing the cap into face-to-face contact with the wafer such that each of the continuous solder beads contacts and surrounds an active area of a corresponding chip portion;

(F) melting the solder to bond the cap to each of the chip portions and thereby form a hermetic seal around the active areas of each of the chip portions; and,

(G) cutting the wafer into individual die.

13. The method of Claim 12, including applying a plurality of spacers on the cap to maintain a desired spacing between the cap and the wafer.

14. The method of Claim 13, wherein step (G) includes cutting away portions of the cap having the spacers applied thereto.

15. The method of Claim 12, wherein step (D) is performed by electroplating a layer of solder material through a pattern mask onto the metalization layer.

16. The method of Claim 15, including the steps of removing the pattern mask and then reflowing the solder beads.

17. A hermetically sealed, wafer level, chip scale package produced by the method of Claim 12.

18. A hermetically sealed, wafer level, chip scale package produced by the method of Claim 13.

19. A hermetically sealed, wafer level, chip scale package produced by the method of Claim 14.

20. A hermetically sealed, wafer level, chip scale package produced by the method of Claim 15.

21. A hermetically sealed, wafer level, chip scale package produced by the method of Claim 16.

22. A hermetically sealed, wafer level, chip scale package, comprising:

a semiconductor chip substrate having an active circuit area;

a cap for protectively covering the active area; and

a solder bead welded to the cap and to the chip substrate, the solder bead completely surrounding and hermetically sealing the active area.

23. The hermetically sealed, wafer level, chip scale package of Claim 22, wherein the cap is silicon.

24. The hermetically sealed, wafer level, chip scale package of Claim 22, wherein the cap is held in spaced relationship to the chip substrate by the solder bead.

25. The hermetically sealed, wafer level, chip scale package of Claim 22, wherein the cap includes a layer of metalization formed thereon, and the solder bead is bonded to the metalization layer.